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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/613,367	07/03/2003	Carsten Ohlhoff	W&B-INF-1850	4886

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EXAMINER
BRITT, CYNTHIA H

ART UNIT	PAPER NUMBER
2138	

DATE MAILED: 06/13/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

PTO-90C (Rev. 10/03)

	Application No.	Applicant(s)
Office Action Summary	10/613,367	OHLHOFF ET AL.
	Examiner	Art Unit	
	Cynthia Britt	2138	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE <u>3</u> MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.
- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**.   2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-11* is/are pending in the application.

    4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-11* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on <u>03 July 2003</u> is/are: a)☒ accepted or b)☐ objected to by the Examiner.

    Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

    Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

    a)☒ All   b)☐ Some * c)☐ None of:

      1.☒ Certified copies of the priority documents have been received.

      2.☐ Certified copies of the priority documents have been received in Application No. _____.

      3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

    * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)

2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
    Paper No(s)/Mail Date _____.

4) ☒ Interview Summary (PTO-413)
    Paper No(s)/Mail Date. *6/8/06* .

5) ☐ Notice of Informal Patent Application (PTO-152)

6) ☐ Other: _____.

DETAILED ACTION

Claims 1-11 are pending in this application.

Response to Arguments

Applicant's arguments filed 3/27/06 have been fully considered but they are not persuasive.

Applicant argues, "One concept of the invention of the instant application is that a number of memory tests can be performed without reading out test result data. In particular, in case of soft error it can occur that an error in a memory cell is detected in one test process and not detected in a following test process. Therefore, conventionally, after each test process test results have to be read out by a tester unit. According to the invention of the instant application, it is not provided that a test process is carried out to test the memory circuit wherein if an error occurs it is provided in a next test process the data which are written in the respective memory cell of the memory circuit are modified such that a following comparison of the written and read out data results in the detection of an error even if the respective memory cell has stored the written data in the following test process correctly. The invention of the instant application allows to carry out a plurality of test processes in the memory circuit without instantaneously reading out the test results and without losing any Information about the occurrence of soft errors detected in any of the test processes."

In general these arguments are unclear specifically the underlined portion.

It is noted that the features upon which applicant relies (i.e., see above) are not recited in the rejected claim(s). Although the claims are interpreted in

light of the specification, limitations from the specification are not read into the

claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

The applicant also argues, "The test circuit according to Dahn does not

include a data change circuit according to the invention of the instant application.

Dahn does not show a data change circuit, which is connected in the data input

line and which is able to change the test data value written into the memory

circuit depending on a result of a comparison performed in a proceeding teat

process. In other words, the changeover device according to Dahn does nothing

more than copying the comparison result into each of the memory banks not

being tested therefore does not change any teat data to be written into the

memory bank to be tested. Moreover, the changeover device of Dahn has no

functionality, which depends on a result of the comparison performed in the

comparator unit since the comparison results are copied into the memory banks

not being tested, i.e. in case of an error and in case of no error."

The examiner would like to point out that the independent claims in the

instant application (claims 1 and 7) fail to articulate what happens to the data 'in

case of no error'. Claim 1 and claim 7 are both silent on this issue. This issue is

not addressed until claim 4 (which would clarify what applicant is intending to

claim). The independent claims fail to recite what type of change is taking place

to the data (correcting the erroneous data, a timing or delay change or merely an

inversion of the data). There are many ways that data can be changed and

without articulating what type of change is taking place, the limitations of this

claim language are very broad. Thus, they would read on the cited reference.

Therefore, the previous rejection will be maintained.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35

U.S.C. 102 that form the basis for the rejections under this section made in this

Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-3, 5, 7, 8, 10, and 11 are rejected under 35 U.S.C. 102(e) as

being anticipated by Dahn U.S. Patent No. 6,539,505.

As per claims 1 and 7, Dahn teaches the claimed method and circuit in

which a test circuit for testing a memory having a data input line for providing test

data to be written to the memory circuit (figure 2 DQ lines column 6 lines 18-21) a

comparator unit comparing expected values received over said data input line

with the test data read from the memory circuit, the test data previously having

been written to the memory circuit over said data input line(column 4 lines 56-64)

and a data change circuit connected between said data input line and the

memory circuit, said data change circuit being controllable depending on a result

of a comparison performed in said comparator unit such that when an error

occurs, further test data can be written to the memory circuit in a manner altered

by said data change circuit. (column 3 lines 40-52 also see claim 1)

As per claims 2, Dahn teaches the expected values correspond to the test data previously written to the memory circuit. (column 2 lines 20-34, column 4 lines 56-66)

As per claims 3, and 5, Dahn teaches the data change circuit is one of a plurality of data change circuits; and said data input line is one of a plurality of data input lines each connected to one of said data change circuits, said data change circuits being controlled by said comparator device such that when the error occurs in a memory area addressed through one of said data input lines, each of said data change circuits is controlled such that the further test data on said plurality of data input lines can be written to the memory circuit in the altered manner, and when the error occurs in the memory area addressed by one of said further data input lines of one of said blocks, said data change circuits for all of said further data input lines of a respective block are controllable such that the further test data on said further data input lines of said respective block can be written in the altered manner to the memory circuit.. (column 3 lines 40-52 also see claim 1, column 6 lines 18-41)

As per claim 8, Dahn teaches writing the altered test data into at least one further memory area after the detection of the error in the memory area, so that the further test data transmitted for the memory area and for the at least one further memory area and the altered test data read therefrom are different. (column 4 lines 56-66)

As per claims 10 and 11, Dahn teaches altering a specific operating parameter of the memory circuit between repeated writing-in and reading-out of the altered test data, and performing a plurality of write/read operations; and outputting error data to an evaluation unit, the error data specifying differences between the further test data transmitted during a last write operation and the altered test data read out during a last read operation. (column 5 lines 6-27)

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* v. *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1.   Determining the scope and contents of the prior art.
2.   Ascertaining the differences between the prior art and the claims at issue.
3.   Resolving the level of ordinary skill in the pertinent art.
4.   Considering objective evidence present in the application indicating obviousness or nonobviousness.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any

inventions covered therein were made absent any evidence to the contrary.

Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor

and invention dates of each claim that was not commonly owned at the time a

later invention was made in order for the examiner to consider the applicability of

35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35

U.S.C. 103(a).

Claims 4, 6, and 9, are rejected under 35 U.S.C. 103(a) as being

unpatentable over Dahn U.S. Patent No. 6,539,505 in view of Morgan et al. U.S.

Patent No. 6,072,737.

As per claim 4, Dahn substantially teaches the claimed circuit in which a

test circuit for testing a memory having a data input line for providing test data to

be written to the memory circuit (figure 2 DQ lines column 6 lines 18-21) a

comparator unit comparing expected values received over said data input line

with the test data read from the memory circuit, the test data previously having

been written to the memory circuit over said data input line(column 4 lines 56-64)

and a data change circuit connected between said data input line and the

memory circuit, said data change circuit being controllable depending on a result

of a comparison performed in said comparator unit such that when an error

occurs, further test data can be written to the memory circuit in a manner altered

by said data change circuit (column 3 lines 40-52 also see claim 1) and inverting

the test data (Column 5 lines 7-12). Not disclosed by Dahn is that the data

change circuit has a controllable exclusive-OR gate which, depending on a

control signal generated by said comparator device, passes the test data in

unaltered form to the memory unit or inverts the test data with an aid of an

exclusive-OR function resulting in the further test data being altered test data.

However, in an analogous art, Morgan et al teach the use of exclusive OR

circuitry dependent on the output of the controller that passes the data through

an exclusive OR function. (Figure 6, elements 28, 505,506, and 304, column 3

lines 14-31). Therefore, it would have been obvious to a person having ordinary

skill in the art at the time this invention was made to have used the XOR circuitry

of Morgan et al. with the change circuit of Dahn. One would have been motivated

to do so in order to identify defective memory circuitry as suggested by Dahn

(column 2 lines 1-4).

As per claim 6, Dahn and Morgan et al. as combined above substantially

teach the claimed circuit where comparison unit has a reset input for driving said

comparison unit to not alter the test data in said data change circuit (Morgan et

al. Figure 9 lines 41-59).

As per claim 9, Dahn and Morgan et al. as combined above substantially

teach the claimed method in which altering the further test data into the altered

test data with an aid of an exclusive-OR function after the detection of the error

(Dahn column 5 lines 6-12, and Morgan et al. Figure 4).

Conclusion

The prior art made of record and not relied upon is considered pertinent to

applicant's disclosure.

U.S. Patent No. 6,691,272   Azim, Syed K.

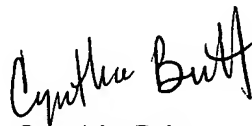This patent teaches a 'change' of the delay type.

The examiner would like to point out that this rejection is not being made final as these issues have been discussed with attorney of record for applicant and no conclusion has been reached as to correction. Therefore, the examiner is awaiting a return call.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Cynthia Britt whose telephone number is 571-272-3815. The examiner can normally be reached on Monday - Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on 571-272-3819. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from

the Patent Application Information Retrieval (PAIR) system. Status information

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PAIR. Status information for unpublished applications is available through

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direct.uspto.gov. Should you have questions on access to the Private PAIR

system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-

free). If you would like assistance from a USPTO Customer Service

Representative or access to the automated information system, call 800-786-

9199 (IN USA OR CANADA) or 571-272-1000.

Cynthia Britt
Examiner
Art Unit 2138